JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

A Boundary Scan Test Vehicle for Direct Chip Attach (DCA) Testing

Heather Parsons

Saverio D'Agostino

Genji Arakaki

Jet Propulsion Laboratory

5/10/1999

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Topics

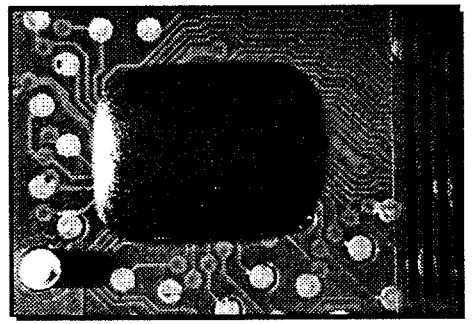
- Background: Direct Chip Attach
- Test Methods
- What is boundary scan and how does it work
- How is it currently being used
- Usefulness to others

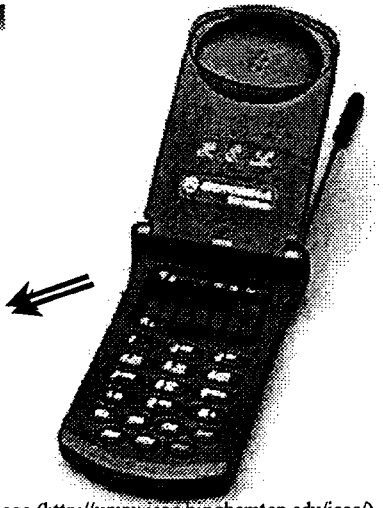
Background: What is Direct Chip Attach?

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

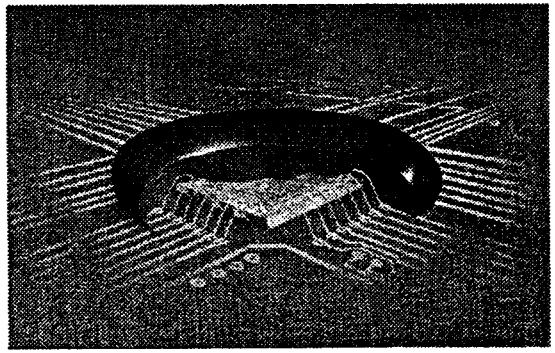
- Equivalent to Chip-On-Board
- Bare die bonded directly to the printed wiring board
- Wire bonded
- Non-Hermetic Packaging
- To validate an encapsulation or passivation technology for New Millenium Deep Space - 2 (DS-2) and other flight projects

Motorola Star-Tac

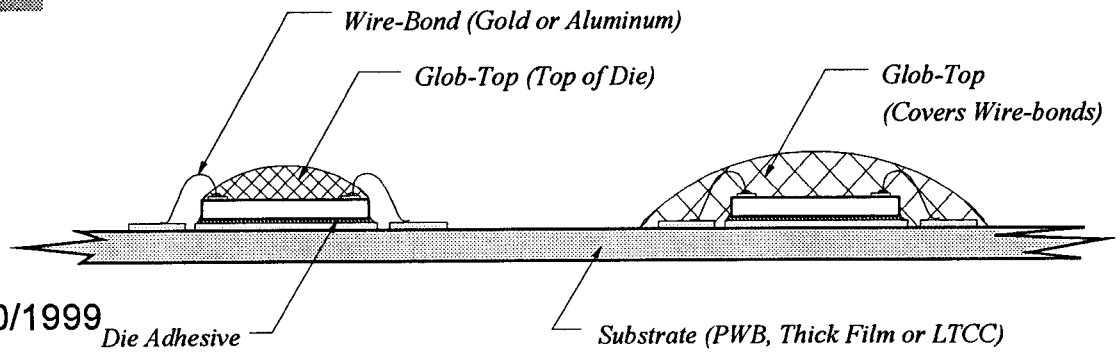




Ref: Binghamton University web page (http://www.ieec.binghamton.edu/ieec/)



Ref: Circuits Assembly, 1996



JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Background:DCA Objectives

- To design a substrate that
  - gives a realistic understanding of how the environment affects powered devices
  - provides information about the reliability of passivation technology
- Span wide range of part types
- Testing
  - Fast
  - Automated
  - Repetitive
  - Log data

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Test Methods

Daisy Chain

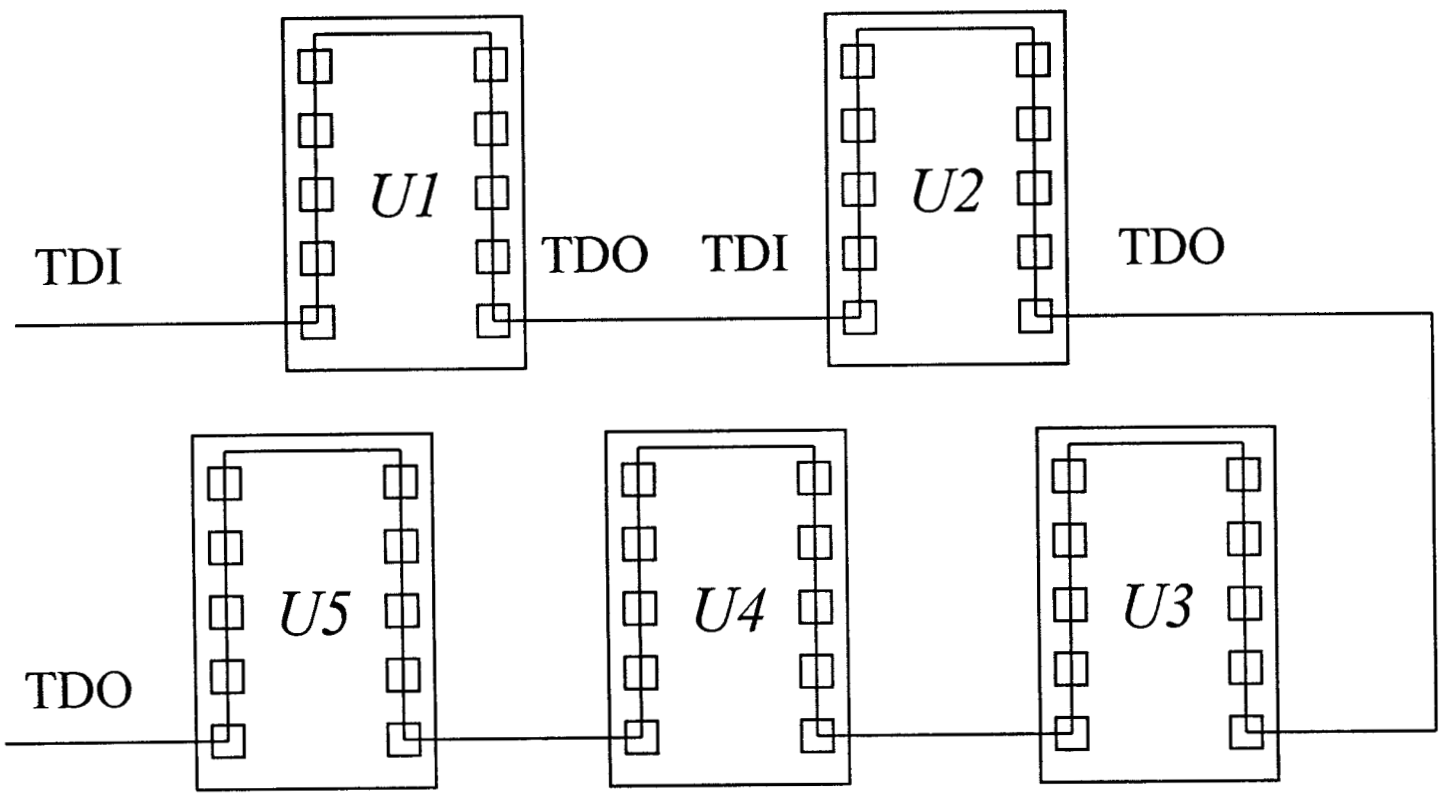
- simple for solder joints or connectors
- non-powered devices
- don't know exactly what interconnect has failed

Boundary Scan

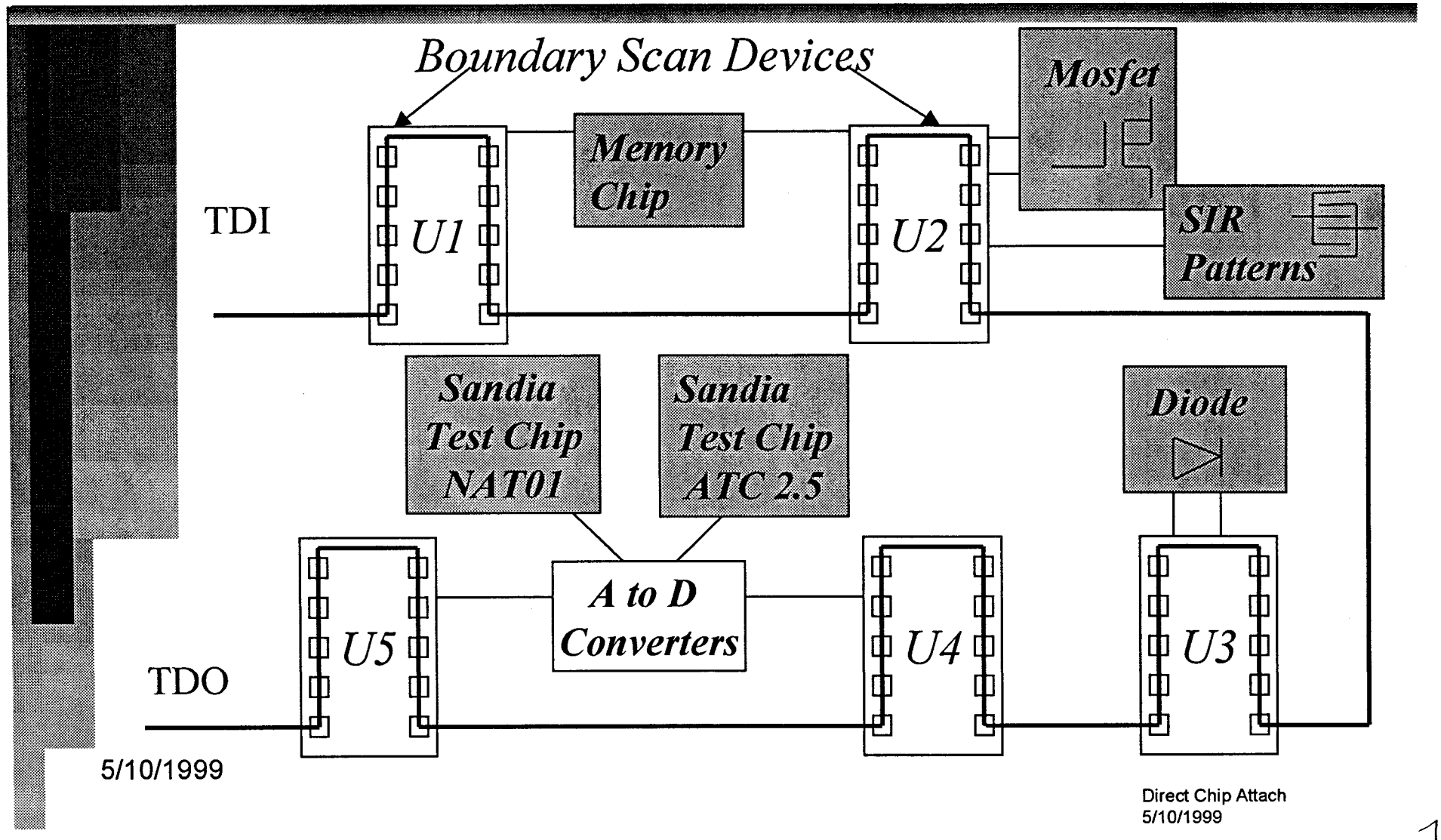
- IEEE Standard (JTAG)
  - Standardized
  - Commercially available
- powered devices
- digital test
- determine failure at interconnect level
  - short
  - open

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Boundary Scan Chip



Board Design



JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Devices on Board

Packaged Parts

- Boundary Scan Chips
- Resistors
- A to D Converters

Bare Die

- A Memory Chip
- Several Schottky Diodes
- MOSFETs (Both N and P Channel)
- Sandia Test Chips
  - ATC 2.5
  - NAT01
- SIR Patterns

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Boundary Scan Test

- *Diodes - Series connected with resistor*
- *Mosfets - N and P channel configured as inverters*
- *SIR Patterns - Voltage divider will show non-zero value if current flows*
- *ATC2.5 / NAT01 - A to D Converters will sense change in voltage divider*

Test of Static Memory (SRAM) by Boundary Scan

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

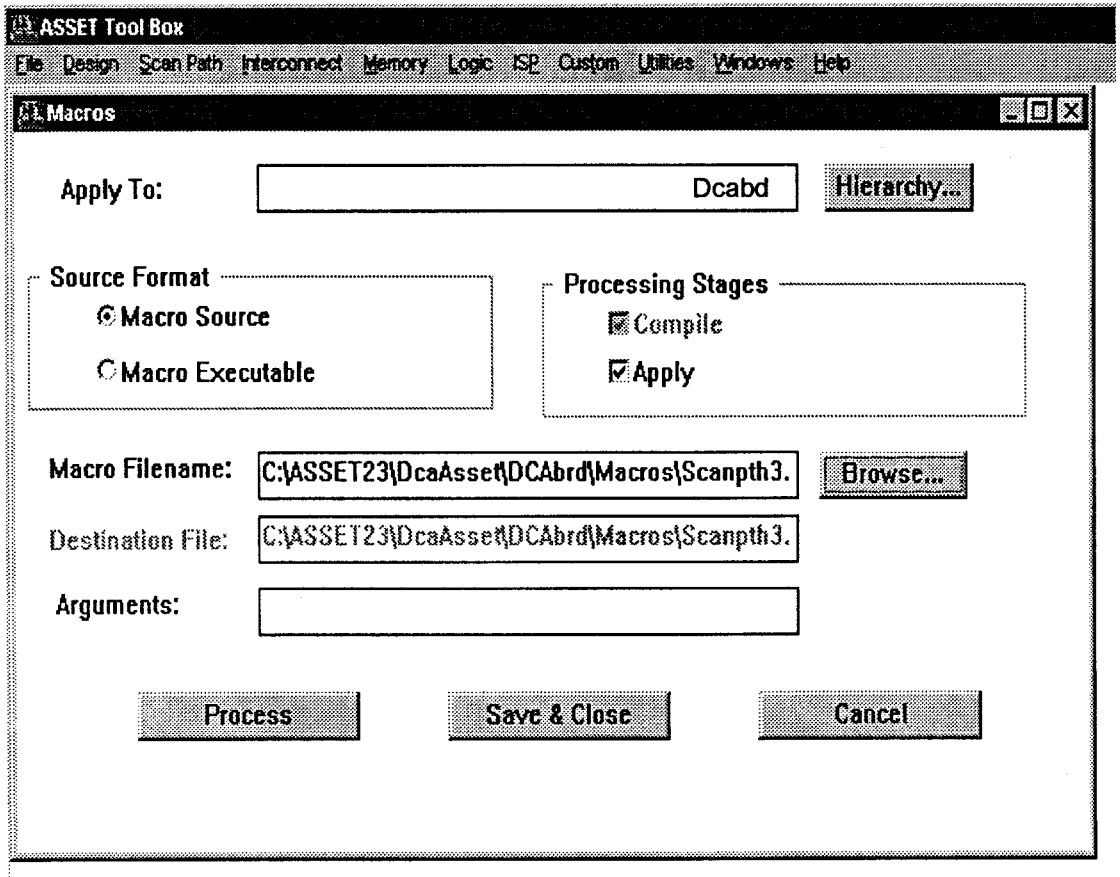
- Boundary Scan used to write to SRAM
  - Boundary Scan Chip 1 feeds addresses
  - Boundary Scan Chip 1 feeds data inputs
- Boundary Scan used to read SRAM
  - Chip 1 feeds addresses
  - Chip 2 reads Data outputs
- Data shifted out - verified

The Boundary Scan Test System

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY

Asset

- Hardware Card
- Interface Pod
- Windows Software



The Boundary Scan Test System

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY

```
Scan Path ATPG: Test results for entity dcabd3.This test detects:
- Stuck-at-0 on the TDI/TDO data path.
- Inoperative TCK.
- Inoperative TMS.
- Incorrect scan path length.

Pattern Is Constant 1
-----------------
Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
Pattern Is Constant 0
-----------------
Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
Pattern Is Constant 0110
-----------------
Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
INFO MAX064: C:\ASSET23\DcaAsset\DCAbrd\Macros\Scanpth3.mac(247) Program ran successfully.
```

- *Uses Macros to program test*
- *Compares test data out to data expected*

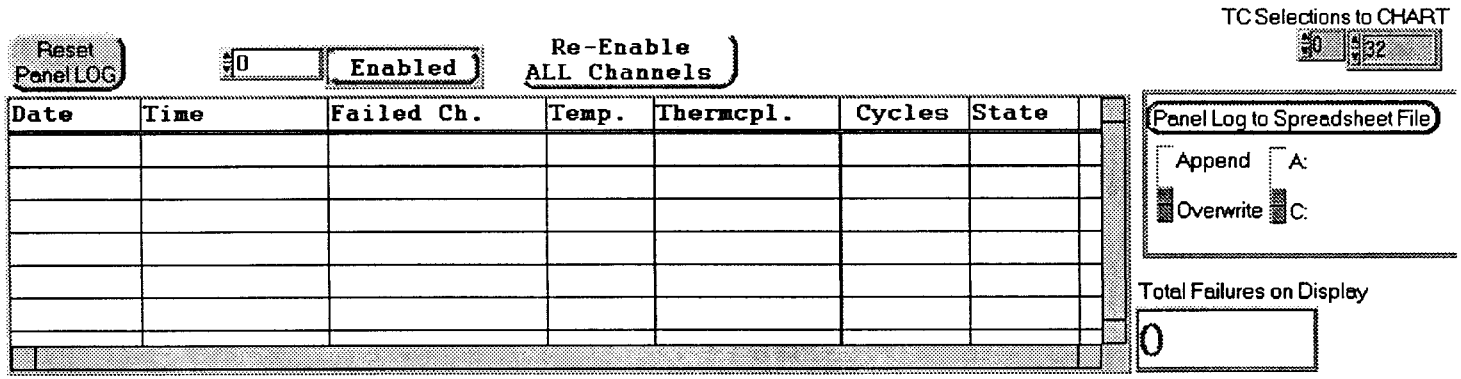
5/10/1999

The Boundary Scan Test System

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY

LabVIEW

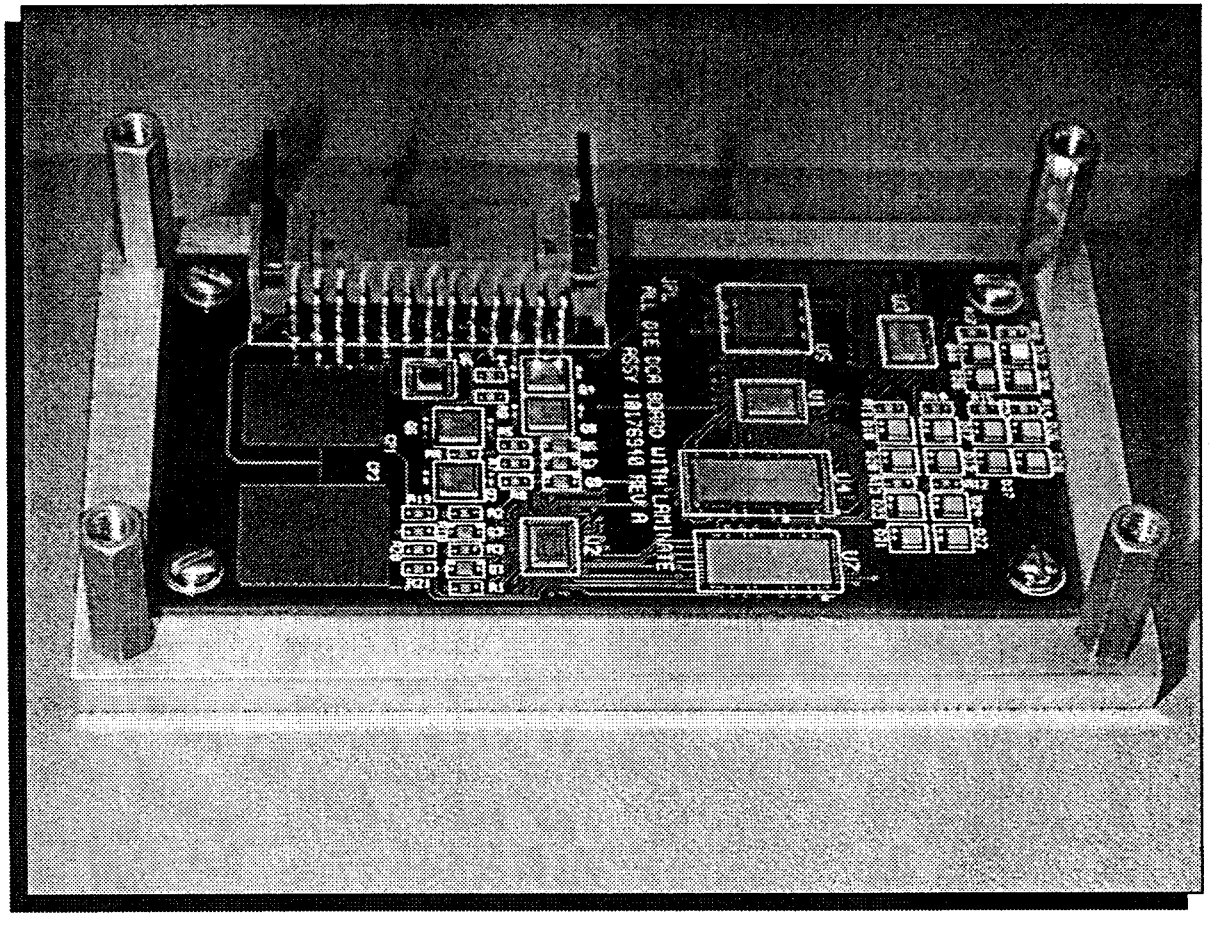
- Logs time, date, and other relevant information when there is a failure
- Continuous testing



JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Successfully able to test

- *diodes*
- *mosfets*
- *SRAM*



5/10/1999

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Future Tasks

- *LabVIEW up and running*
- *Continuous testing in thermal and HAST chambers*
- *Testing all different types of new Packaging technologies*

JPL
JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE
OF TECHNOLOGY

Summary

- *Boundary Scan use for DCA*
  - *test at interconnect level*
  - *automated testing that logs failures*
- *Boundary Scan as a valuable resource to testing new technologies*